PATENT
8733.947.00

UNITED STATES PATENT APPLICATION

OF

HUN JEOUNG

AND

HONG SOO KIM

FOR

LIQUID CRYSTAL DISPLAY AND METHOD OF DRIVING THE SAME

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, N.W.
WASHINGTON, D.C. 20006
Tel: (202) 496-7500
Fax: (202) 496-7756

[0001] This application claims the benefit of the Korean Patent Application No. 2002-77378 filed on December 6, 2002, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to liquid crystal display (LCD) devices. More particularly, the present invention relates to a LCD device and a method of driving the same, wherein generation of a horizontal stripe phenomenon may be prevented.

Description of the Related Art

[0003] Generally, liquid crystal display (LCD) devices control light transmittance characteristics of liquid crystal material in accordance with applied electric fields. Accordingly, LCD devices typically include an LCD panel having a plurality of liquid crystal cells arranged in a matrix pattern, and drive circuits to drive the plurality of liquid crystal cells.

[0004] Figure 1 illustrates a related art liquid crystal display (LCD) device.

[0005] Referring to Figure 1, the related art includes an LCD panel 12 having a plurality of liquid crystal cells 20 arranged in a matrix pattern, a gate diver 14 for driving a plurality of gate lines GL1 to GLn, a data driver 16 for driving a plurality of

data lines DL1 to DLm, and a timing controller 18 for controlling the gate and data drivers 14 and 16, respectively. The LCD panel 12 further includes a plurality of thin film transistors (TFTs) formed at crossings of the plurality of gate and data lines GL1 to GLn and DL1 to DLm, respectively, wherein each of the TFTs is connected to a corresponding liquid crystal cell 20.

[0006] Upon driving the plurality of liquid crystal cells 20, the gate driver 14 sequentially applies scan signals to the plurality of gate lines GL1 to GLn to sequentially drive rows of liquid crystal cells 20. Accordingly, the scan signals include gate high and low voltages (VGH) and (VGL), respectively. Whenever the gate high voltage (VGH) is applied to a gate line (GL), TFTs within the driven row of liquid crystal cells are turned on and pixel signals, applied by the data driver 16 to each of the data lines DL1 to DLm, are transmitted to the driven row of liquid crystal cells 20. Whenever the gate low voltage (VGL) is applied to a gate line (GL), TFTs within the driven row of liquid crystal cells 20 are turned off, wherein a voltage corresponding to a pixel signal remains charged within the liquid crystal cell 20.

[0007] Each liquid crystal cell 20 can be equivalently represented as a liquid crystal capacitor (Clc) including a common electrode capacitively coupled to a pixel electrode by liquid crystal material having anisotropic dielectric properties, wherein the pixel electrode is connected to a TFT. Each liquid crystal cell 20 further includes a storage capacitor (Cst) formed between a pixel electrode and a pre-stage gate line for

retaining a voltage associated with a pixel signal until a subsequent pixel signal is charged to the liquid crystal cell 20. Once a pixel signal is applied from a data line (DL), a turned-on TFT applies a voltage associated with the pixel signal to the pixel electrode to generate electric field between the pixel and common electrodes. In response to the generated electric field, a molecular orientation of the liquid crystal material is manipulated such that light transmittance characteristics of the liquid crystal cell are controlled. Moreover, gray scale values of light are realized by the liquid crystal cell by adjusting the pixel signal voltage.

[0008] The gate driver 14 sequentially applies the gate high voltage (VGH) to the plurality of gate lines GL1 to GLn in response to gate control signals (GSP, GSC, GOE) outputted from the timing controller 18. More specifically, the gate driver 14 generates a shift pulse by shifting a gate start pulse (GSP) in accordance with a gate shift pulse (GSC). Next, the gate driver 14 applies the gate high voltage (VGH) to a predetermined gate line (GL) during each horizontal period in response to the gate shift pulse (GSC). During operation, the gate driver 14 applies the gate high voltage (VGH) only during an enable period of a gate output enable signal (GOE). During periods of time when the gate high voltage (VGH) is not applied, however, the gate driver 14 applies the gate low voltage (VGL) to the gate lines GL1 to GLn.

[0009] The data driver 16 applies pixel signals, specific for each gate line to which the gate high voltage (VGH) is applied, simultaneously to each of the data lines

DL1 to DLm in response to data control signals (SSP, SSC, SOE, POL) outputted from the timing controller 18. More specifically, the data driver 16 generates a sampling signal by shifting a source start pulse (SSP) in accordance with a source shift clock (SSC). Next, the data driver 16 sequentially receives and latches digital pixel data (R,G,B) outputted from the timing controller 18 in response to the sampling signal. The data driver 16 then converts the digital pixel data (R,G,B), latched in correspondence with the gate line to which the gate high voltage (VGH) is applied, into analog pixel signals and applies the analog pixel signals to the data lines DL1 to DLm during the enable period of the source output enable signal (SOE). More specifically, the data driver 16 converts the digital pixel data (R,G,B) into analog pixel signals using gamma signals outputted from a gamma voltage generator (not shown). The data driver 16 also converts the digital pixel data (R,G,B) into positive and negative polarity pixel signals in response to a polarity control signal (POL). For example, in response to the polarity control signal (POL), the data driver 16 inverts the polarity of the pixel signal based on a columnar arrangement of the liquid crystal cells 20 to drive the liquid crystal display panel 12 according to a dot inversion system.

[0010] As mentioned above, the timing controller 18 controls the gate and data drivers 14 and 16 by generating the gate control signals (GSP, GSC, GOE) and the data control signals (SSP, SSC, SOE, POL), respectively. Additionally, the timing controller 18 arranges the pixel data (R,G,B) and applies the arranged digital pixel data

to the data driver 16.

[0011] As described above, liquid crystal cells 20 within the related art LCD display can be driven using an inversion driving method such as a frame inversion, line (column) inversion, or dot inversion method to improve a picture quality of the LCD device. Compared to other inversion driving methods, the dot inversion driving method provides an excellent picture quality. However, and as shown with reference to Figure 2, use of the dot inversion driving method can generate defects, such as horizontal stripes, within the LCD panel 12. As described in greater detail below, the horizontal stripe phenomenon occurs due to the presence of first and second parasitic capacitors Cdp1 and Cdp2 formed between pixel electrodes 20 of liquid crystal cells A and B and preceding and succeeding ones of adjacent data lines (e.g., data lines DLk and DLk+1).

[0012] The horizontal stripe phenomenon, generated when the liquid crystal display panel is driven according to the dot inversion driving method, will now be explained in greater detail with reference to Figures 3 to 5.

[0013] Figure 3 illustrates charging characteristics of vertically adjacent liquid crystal cells with respect to pixel signals applied to the k^{th} data line shown in Figure 2. Figure 4 illustrates charging characteristics of vertically adjacent liquid crystal cells with respect to pixel signals applied to the $(k+1)^{th}$ data line shown in Figure 2. Figure 5 illustrates charging characteristics of vertically adjacent liquid crystal cells

with respect to pixel signals applied to the k^{th} and $(k+1)^{th}$ data lines shown in Figure 2.

[0014] Referring to Figures 2 to 5, during a first horizontal period, a first pixel signal (-Vp), having a negative polarity (-) with respect to the common voltage Vcom, is applied to the kth data line (DLk) while a first pixel signal (+Vp), having a positive polarity (+) with respect to the common voltage Vcom is applied to the $(k+1)^{th}$ data line (DLk+1). The brightness level represented by the first positive polarity pixel signal (+Vp) is relatively higher than the brightness level represented by the first negative polarity pixel signal (-Vp). Simultaneously with the application of the first negative and positive polarity pixel signals -Vp and +Vp, a first thin film transistor (TFT1), connected to the first gate line (GL1), is turned on in response to a scan pulse (not shown) applied to the first gate line (GL1). Accordingly, a first negative pixel voltage Vp1, associated with the first negative polarity pixel signal (-Vp), is charged to the first liquid crystal cell (A) connected to the first gate line (GL1) from the kth data line (DLk).

[0015] Subsequently, during a second horizontal period (H2), a second pixel signal (+Vp), having a positive polarity (+) with respect to the common voltage Vcom, is applied to the kth data line (DLk) while a second pixel signal (-Vp), having a negative polarity (-) with respect to the common voltage Vcom is applied to the $(k+1)^{th}$ data line (DLk+1). The brightness level represented by the second negative polarity pixel signal (-Vp) is relatively higher than the brightness level represented by the

second positive polarity pixel signal (+Vp). Simultaneously with the application of the second positive and negative polarity pixel signals +Vp and -Vp, a second thin film transistor (TFT2), connected to the second gate line (GL2), is turned in response to a scan pulse (not shown) applied to the second gate line (GL2). Accordingly, a second positive pixel voltage Vp2, associated with the second positive polarity pixel signal (+Vp), is charged to the second liquid crystal cell (B), connected to the second gate line (GL2), from the k^{th} data line (DLk).

[0016] As a result of driving the related art LCD panel as described above, the first negative pixel voltage Vp1 is capacitively affected by the second positive polarity pixel signal (+Vp) applied to the k^{th} data line (DLk) via the first parasitic capacitor (Cdp1) and by the second negative polarity pixel signal -Vp applied to the $(k+1)^{th}$ data line (DLk+1) via the second parasitic capacitor (Cdp2) during the second horizontal period (H2). Accordingly, a value of the first negative pixel voltage Vp1 changes during the second horizontal period (H2). Since an absolute value of the second negative polarity pixel signal -Vp applied to the $(k+1)^{th}$ data line (DLk+1) is relatively large, the capacitance of the second parasitic capacitor (Cdp2) is also relatively large, thereby increasing the magnitude of the first negative pixel voltage Vp1 within the first liquid crystal cell (A).

[0017] Moreover, during a third horizontal period (H3), a third negative polarity pixel signal (-Vp) is applied to the k^{th} data line (DLk) to charge a third liquid

crystal cell (not shown) while a third positive polarity pixel signal (+Vp) is applied to the $(k+1)^{th}$ data line (DLk+1). The brightness level represented by the third positive polarity pixel signal (+Vp) is relatively higher than the brightness level represented by the third negative polarity pixel signal (-Vp). Accordingly, the first negative pixel voltage Vp1 and the second positive pixel voltage Vp2 are both capacitively affected by the third negative and positive polarity pixel signals -Vp and +Vp respectively applied to the k^{th} and $(k+1)^{th}$ data lines (DLk) and (DLk+1), respectively, via the first and second parasitic capacitors Cdp1 and Cdp2, respectively, during the third horizontal period (H3). Accordingly, a value of the first negative and second positive pixel voltages Vp1 and Vp2 change during the third horizontal period (H3). Since an absolute value of the third positive polarity pixel signal +Vp applied to the $(k+1)^{th}$ data line (DLk+1) is relatively large, the capacitance of the second parasitic capacitor (Cdp2) is also relatively large, thereby positively decreasing the magnitude of the first negative pixel voltage Vp1 and positively increasing the magnitude of the second positive pixel voltage Vp2.

[0018] As can be seen from the discussion above, the various positive and negative polarity pixel signals, charged within each liquid crystal cell, capacitively affect existing positive and negative pixel voltages, previously charged via the k^{th} and $(k+1)^{th}$ data lines (DLk) and (DLk+1) through the first and second parasitic capacitors Cdp1 and Cdp2 within each liquid crystal cell. Moreover, due to the presence of the

aforementioned polarity control signals (POL) applied to the k^{th} and $(k+1)^{th}$ data lines (DLk) and (DLk+1), the polarity of the capacitance within the parasitic capacitors (Cdp1 and Cdp2) is inverted during each horizontal period (H). As a result, the various pixel voltages charged within each liquid crystal cell can become offset.

[0019] During the data apply period (DAP) of a first frame (1F), pixel signals are applied to the k^{th} and $(k+1)^{th}$ data lines (DLk and DLk+1) in accordance with the dot inversion method. Due to the aforementioned offset, changes in first and second effective voltages (EVa and EVb) of the first and the second liquid crystal cells A and B, respectively, are substantially the same.

[0020] During a blanking period (BP) succeeding the data apply period (DAP), however, the k^{th} and $(k+1)^{th}$ data lines (DLk and DLk+1) are placed in a floating state wherein the first and second liquid crystal cells A and B are capacitively coupled with pixel signals applied during the n^{th} horizontal period (Hn) of n number of horizontal periods. Accordingly, values of the first (negative) and second (positive) pixel voltages Vp1 and Vp2 associated with the n^{th} horizontal period are maintained during the blanking period.

[0021] For example, during the n^{th} horizontal period, an n^{th} negative pixel signal is applied to the k^{th} data line (DLk) while an n^{th} positive pixel signal is applied to the $(k+1)^{th}$ data line (DLk+1). The brightness level represented by the n^{th} positive polarity pixel signal (+Vp) is relatively higher than the brightness level represented by

the n^{th} negative polarity pixel signal (-Vp). Accordingly, the n^{th} negative and positive pixel signals are applied to the k^{th} and $(k+1)^{th}$ data lines (DLk and DLk+1), respectively, during the blanking period (BP). As a result, the first (negative) and second (positive) pixel voltages Vp1 and Vp2 are capacitively affected by the n^{th} pixel signals. More specifically, the magnitude of the first negative pixel voltage Vp1 is positively decreased a first amount due to the first parasitic capacitor (Cpd1) while the magnitude of the first negative pixel voltage Vp1 is negatively increased a second amount, greater than the first amount, due to the second parasitic capacitor (Cpd2). Further, the magnitude of the positive pixel voltage Vp2 is negatively decreased a first amount due to the first parasitic capacitor (Cpd1) while the magnitude of the first negative pixel voltage Vp1 is positively increased a second amount, greater than the first amount, due to the second parasitic capacitor (Cpd2). Since an absolute value of the first negative pixel voltage (Vp1) decreases during the blanking period (BP) while an absolute value of the second positive pixel voltage (Vp2) increases during the blanking period (BP), the intensity to which the first liquid crystal cell (A) transmits light differs compared to the intensity to which the second liquid crystal cell (B) transmits light.

[0022] Based on the values of the pixel signals Vp applied to the first and second liquid crystal cells (A) and (B) via the k^{th} data line DLk, and based on the first (negative) and second (positive) pixel voltages Vp1 and Vp2, respectively, charged

within the first and second liquid crystal cells (A) and (B), respectively, during the blanking period (BP), the effective pixel voltages EVa and EVb of the first and second liquid crystal cells (A) and (B), respectively, are determined by the following equations:

$$EVa = (1-t) \times Vp + t \times Vp1$$

$$EVb = (1-t) \times Vp + t \times Vp2,$$

wherein t represents the duration of the blanking period (BP) within of one frame period (1F) and (1-t) represents the duration of the data apply period (DAP) within one frame period (1F).

[0023] Accordingly, the intensity to which an i^{th} horizontal having the first liquid crystal cell (A) line transmits light differs compared to the intensity to which an $(i+1)^{th}$ horizontal line having the second liquid crystal cell (B) transmits light during the blanking period (BP) and the horizontal stripe phenomenon is generated.

[0024] Referring to Figure 6, the effect of the horizontal stripe phenomenon is similar to the effect of displaying a green (G) pattern along a vertical direction. Accordingly, the picture quality in the related art LCD device is deteriorated. Moreover, the effect of the horizontal stripe phenomenon becomes more apparent as the duration of the blanking period within the frame increases, as the difference between absolute values of the pixel signals supplied to adjacent ones of data lines increases, and as differences in the capacitance values of the first and second parasitic

capacitors Cdp1 and Cdp2 increases.

SUMMARY OF THE INVENTION

[0025] Accordingly, the present invention is directed to a liquid crystal display and a method of driving the same, wherein generation of the horizontal stripe phenomenon may be prevented, that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0026] An advantage of the present invention provides a dummy pixel signal representing an identical brightness level to data lines during a blanking period to thereby prevent generation of the horizontal stripe phenomenon.

[0027] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0028] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a liquid crystal display device may for example, include a liquid crystal display panel having gate lines, data lines crossing the gate lines, and liquid crystal cells formed at crossings of the gate and data lines; a liquid crystal display panel driver for driving the gate and

data lines, wherein effective pixel signals are applied to the liquid crystal cells during a data apply period and wherein dummy pixel signals have identical brightness levels are applied to the liquid crystal cells during a blanking period.

[0029] In one aspect of the present invention, the liquid crystal display panel driver may, for example, include a gate driver for sequentially driving the gate lines during the data apply period; and a data driver for applying the effective pixel signals to the data lines during the data apply period and for applying the dummy pixel signals to the data lines during the blanking period, wherein the data lines are placed in a floating state thereafter.

[0030] In another aspect of the present invention, the data driver may convert effective digital pixel data into the effective pixel signals during the data apply period, wherein the effective pixel signals are analog signals; convert dummy digital pixel data into the dummy pixel signals during the blanking period; apply the effective pixel signals during the data apply period; and apply the dummy pixel signals during the blanking period.

[0031] In still a further aspect of the present invention, the effective and dummy digital pixel data may be applied from a timing controller, wherein the timing controller controls the gate and data drivers.

[0032] In yet another aspect of the present invention, the data driver may invert the polarity of effective pixel signals applied to adjacent ones of data lines

during the data apply period; and invert the polarity of dummy pixel signals applied to adjacent ones of data lines during the blanking period.

[0033] In still a further aspect of the present invention, the data driver may invert the polarity of effective pixel signals applied to a data line during sequential ones of n horizontal periods (where n is an integer) during the data apply period.

[0034] In yet a further aspect of the present invention, the dummy pixel signals applied during the blanking period may include a white signal.

[0035] According to principles of another aspect of the present invention, a method of driving a liquid crystal display may, for example, include applying effective pixel signals to data lines of liquid crystal cells within a liquid crystal display panel during an effective data apply period; and applying dummy pixel signals to the data lines during a blanking period, wherein brightness levels of the dummy pixel signals may be substantially identical.

[0036] In one aspect of the present invention, the driving method may further include applying dummy pixel signals to the data lines during the blanking period, wherein the data lines are in a floating state thereafter.

[0037] In another aspect of the present invention, the polarity of effective pixel signals applied to adjacent ones of data lines may be inverted during the data apply period and the polarity of dummy pixel signals applied to adjacent ones of data lines may be inverted during the blanking period.

[0038] In still another aspect of the present invention, the polarity of effective pixel signals applied to a data line during sequential ones of n horizontal periods (n is an integer) during the data apply period may be inverted.

[0039] In yet another aspect of the present invention, the dummy pixel signals may be applied as white signals.

[0040] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0041] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0042] In the drawings:

[0043] Figure 1 schematically illustrates a related art liquid crystal display (LCD) device;

[0044] Figure 2 illustrates parasitic capacitors of vertically adjacent liquid crystal cells within the related art LCD device shown in Figure 1;

[0045] Figure 3 illustrates charging characteristics of vertically adjacent liquid

crystal cells with respect to pixel signals applied to the k^{th} data line shown in Figure 2;

[0046] Figure 4 illustrates charging characteristics of vertically adjacent liquid crystal cells with respect to pixel signals applied to the $(k+1)^{th}$ data line shown in Figure 2;

[0047] Figure 5 illustrates charging characteristics of vertically adjacent liquid crystal cells with respect to pixel signals applied to the k^{th} and $(k+1)^{th}$ data lines shown in Figure 2;

[0048] Figure 6 illustrates the horizontal stripe phenomenon generated when a predetermined pattern is displayed by the liquid crystal display panel shown in Figure 1;

[0049] Figure 7 schematically illustrates an LCD device according to principles of the present invention; and

[0050] Figure 8 illustrates charging characteristics of vertically adjacent liquid crystal cells with respect to pixel signals applied to the second and third data lines shown in Figure 7.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0051] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0052] Figure 7 schematically illustrates a liquid crystal display (LCD) device

according to principles of the present invention.

[0053] Referring to Figure 7, the LCD of the present invention may, for example, include an LCD panel 22 having a plurality of liquid crystal cells 30 arranged in a matrix pattern, a gate diver 24 for driving a plurality of gate lines GL1 to GLn, a data driver 26 for applying effective pixel signals to data lines DL1 to DLm during a data apply period (DAP) and for applying dummy pixel signals to data lines DL1 to DLm during a blanking period (BP); and a timing controller 28 for controlling the gate and data drivers 24 and 26, respectively. In one aspect of the present invention, brightness levels of all of the dummy pixel signals may be substantially identical.

[0054] The LCD panel 22 may further include a plurality of thin film transistors (TFTs) arranged at crossings of the plurality of gate lines GL1 to GLn and the plurality of data lines DL1 to DLm, wherein each of the plurality of TFTs may be connected to a respective liquid crystal cell 30.

[0055] Upon driving the plurality of liquid crystal cells 30, the gate driver 24 may sequentially apply scan signals to the plurality of gate lines GL1 to GLn to sequentially drive rows of liquid crystal cells 30. Accordingly, scan signals may include gate high and low voltages (VGH) and (VGL), respectively. Whenever the gate high voltage (VGH) is applied to a gate line (GL), TFTs within the driven row of liquid crystal cells 30 may be turned on and pixel signals, applied by the data driver 26

applied to each of the data lines DL1 to DLm, are transmitted to the driven row of liquid crystal cells 30. Whenever the gate low voltage (VGL) is applied to a gate line (GL), TFTs within the driven row of liquid crystal cells 30 are turned off, wherein voltages corresponding to the applied pixel signals remain charged within the liquid crystal cells 30.

[0056] According to principles of the present invention, each liquid crystal cell 30 may be equivalently represented as a liquid crystal capacitor (Clc) including a common electrode capacitively coupled to a pixel electrode by liquid crystal material having anisotropic dielectric properties, wherein the pixel electrode is connected to a corresponding TFT. Further, each pixel electrode is capacitively coupled to a preceding adjacent data line via a first parasitic capacitor (Cdp1) while each pixel electrode is capacitively coupled to a succeeding adjacent data line via a second parasitic capacitor (Cdp2). In one aspect of the present invention, the conductors of each parasitic capacitor comprise the adjacent data line and the pixel electrode while the insulator of each parasitic capacitor may include an insulating film, air, or the like. Still further, each liquid crystal cell 30 may further include a storage capacitor (Cst) formed between a pixel electrode and a pre-stage gate line, wherein the storage capacitor (Cst) retains a voltage associated with a pixel signal until a subsequent pixel signal is charged to the liquid crystal cell 30. Once a pixel signal is applied from a data line (DL), a turned-on TFT may apply a voltage associated with the pixel signal to the

pixel electrode to generate electric field between the pixel and common electrodes. In response to the generated electric field, a molecular orientation of the liquid crystal material may be manipulated such that light transmittance characteristics of the liquid crystal cell may be controlled. Moreover, gray scale values of light may be realized by the liquid crystal cell by adjusting the pixel signal voltage.

[0057] According to principles of the present invention, the gate driver 24 may sequentially apply the gate high voltage (VGH) to the plurality of gate lines GL1 to GLn in response to gate control signals (GSP, GSC, GOE) outputted from the timing controller 28. More specifically, the gate driver 24 may generate the shift pulse by shifting a gate start pulse (GSP) in accordance with the gate shift pulse (GSC). Next, the gate driver 24 may apply the gate high voltage (VGH) to a predetermined gate line (GL) during each horizontal period in response to the gate shift pulse (GSC). During operation, the gate driver 24 may apply the gate high voltage (VGH) only during an enable period of a gate output enable signal (GOE). During periods of time when the gate high voltage (VGH) is not applied, however, the gate driver 24 may apply the gate low voltage (VGL) to the gate lines GL1 to GLn.

[0058] According to principles of the present invention, the data driver 26 may apply effective pixel signals, specific for each gate line to which the gate high voltage (VGH) is applied, simultaneously to each of the data lines DL1 to DLm during an effective data apply period (DAP) in response to data control signals (SSP, SSC, SOE,

POL) outputted by the timing controller 28. More specifically, the data driver 26 may generate a sampling signal by shifting a source start pulse (SSP) in accordance with a source shift clock (SSC) during the data apply period (DAP). Next, the data driver 26 may sequentially receive and latch digital pixel data (R,G,B) outputted from the timing controller 28 in response to the sampling signal. The data driver 26 may then convert the digital pixel data (R,G,B), latched in correspondence with the gate line to which the gate high voltage (VGH) is applied, into analog pixel signals and apply the effective pixel signals to the data lines DL1 to DLm during the enable period of the source output enable signal (SOE). More specifically, the data driver 26 may convert the digital pixel data (R,G,B) into analog pixel signals using gamma signals outputted from a gamma voltage generator (not shown). The data driver 26 may also convert the digital pixel data (R,G,B) into positive and negative pixel signals in response to a polarity control signal (POL). For example, in response to the polarity control signal (POL), the data driver 26 inverts the polarity of the pixel signal based on a columnar arrangement of the liquid crystal cells 40 to drive the liquid crystal display panel 22 according to a dot inversion system.

[0059] Further, the data driver 26 may also apply dummy pixel signals simultaneously to each of the data lines DL1 to DLm during a blanking period (BP). In one aspect of the present invention, brightness levels of the dummy pixel signals may be substantially identical. In another aspect of the present invention, the

blanking period (BP) may succeed the data apply period (DAP). In still another aspect of the present invention, the dummy pixel signals may, for example, include white pixel signals. In yet another aspect of the present invention, the data driver 26 may receive digital dummy pixel data outputted from the timing controller 28 during the blanking period (BP). The data driver 26 may then convert the digital dummy pixel data into analog dummy pixel signals and apply the dummy pixel signals to the data lines DL1 to DLm. After applying the dummy pixel signals to the data lines, the data lines DL1 to DLm may be induced into a floating state until the next data apply period (DAP) is initiated. In a first alternate aspect of the present invention, however, the data driver 26 may receive the analog dummy pixel signals directly from the gamma voltage generator during the blanking period (BP). In a second alternate aspect of the present invention, a dummy pixel signal generator may be provided to apply analog dummy pixel signals to all data lines DL1 to DLm.

[0060] As mentioned above, the timing controller 28 may control the gate and data drivers 24 and 26 by generating the gate control signals (GSP, GSC and GOE) and the data control signals (SSP , SSC , SOE and POL), respectively. Additionally, the timing controller 28 may arrange the digital pixel data (R ,G, and B) and applies the arranged digital pixel data to the data driver 26. In one aspect of the present invention, the timing controller 28 may apply dummy pixel data, specific for each gate line to which the gate high voltage (VGH) is applied, to the data driver 26 during the

blanking period (BP) if the dummy pixel signals are not generated by data driver 26.

[0061] According to principles of the present invention, the LCD display may apply effective pixel signals to the data lines DL1 to DLm during an effective data apply period (DAP) of one frame (1F). Subsequently, the LCD display may apply dummy pixel signals to the data lines DL1 to DLm during a blanking period (BP) of the frame (1F) after which, the data lines DL1 to DLm may be induced into a floating state until the next data apply period (DAP) is initiated in a next frame. According to principles of the present invention, the dummy pixel signals applied to the data lines DL1 to DLm during the blanking period (BP) have substantially identical absolute voltage values, representing substantially identical brightness levels. As a result, the absolute capacitance values of the first and second parasitic capacitors (Cdp1 and Cdp2) within all of the liquid crystal cells 30 of the LCD panel 22 are substantially identical. When the absolute capacitance values of the first and second parasitic capacitors (Cdp1 and Cdp2) are the same for all of the liquid crystal cells 30 within the LCD panel 22, the aforementioned horizontal stripe phenomenon can be substantially prevented from being generated during the blanking period.

[0062] Figure 8 illustrates charging characteristics of vertically adjacent liquid crystal cells with respect to pixel signals applied to the second and third data lines shown in Figure 7.

[0063] Referring to Figure 8, during a first horizontal period (H1), a first

effective pixel signal (-Vp), having a negative polarity (-) with respect to the common voltage Vcom, may be applied to the second data line (DL2) while a first effective pixel signal (+Vp), having a positive polarity (+) with respect to the common voltage Vcom may be applied to the third data line (DL3). The brightness level represented by the first positive polarity effective pixel signal (+Vp) is relatively higher than the brightness level represented by the first negative polarity effective pixel signal (-Vp). Simultaneously with the application of the first negative and positive polarity effective pixel signals -Vp and +Vp, a first thin film transistor (TFT1), connected to the first gate line (GL1), may be turned on in response to a scan pulse (not shown) applied to the first gate line (GL1). Accordingly, a first negative pixel voltage Vp1, associated with the first negative polarity effective pixel signal (-Vp), may be charged to the first liquid crystal cell (C) connected to the first gate line (GL1) from the second data line (DL2).

[0064] Subsequently, during a second horizontal period (H2), a second effective pixel signal (+Vp), having a positive polarity (+) with respect to the common voltage Vcom, may be applied to the second data line (DL2) while a second effective pixel signal (-Vp), having a negative polarity (-) with respect to the common voltage Vcom may be applied to the third data line (DL3). The brightness level represented by the second negative polarity effective pixel signal (-Vp) is relatively higher than the brightness level represented by the second positive polarity effective pixel signal

(+Vp). Simultaneously with the application of the second positive and negative polarity effective pixel signals +Vp and -Vp, a second thin film transistor (TFT2), connected to the second gate line (GL2), is turned in response to a scan pulse (not shown) applied to the second gate line (GL2). Accordingly, the second liquid crystal cell (C) is charged the second positive polarity effective pixel signal +Vp via the second data line (DL2). Accordingly, a second positive pixel voltage Vp2, associated with the second positive polarity pixel signal (+Vp), is charged to the second liquid crystal cell (D), connected to the second gate line (GL2), from the second data line (DL2).

[0065] As a result of driving the LCD panel 22 as described above, a first negative pixel voltage Vp1 may be capacitively affected by the second positive polarity effective pixel signal (+Vp) applied to the second data line (DL2) via the first parasitic capacitor (Cdp1) arranged between the pixel electrode and the second data line) and by the second negative polarity effective pixel signal (-Vp) applied to the third data line (DL3) via a second parasitic capacitor (Cdp2) arranged between the pixel electrode and the third data line during the second horizontal period (H2). Accordingly, a value of the first negative pixel voltage Vp1 changes during the second horizontal period (H2). Since an absolute value of the second negative polarity effective pixel signal (-Vp) applied to the third data line (DL3) is relatively large, the capacitance of the second parasitic capacitor (Cdp2) is also relatively large, thereby

increasing the magnitude of the first negative pixel voltage Vp1 within the first liquid crystal cell (C).

[0066] Moreover, during a third horizontal period (H3), a third negative polarity effective pixel signal (-Vp) may be applied to the second data line (DL2) to charge a third liquid crystal cell (not shown) while a third positive polarity effective pixel signal (+Vp) may be applied to the third data line (DL3). The brightness level represented by the third positive polarity effective pixel signal (+Vp) may be relatively higher than the brightness level represented by the third negative polarity effective pixel signal (-Vp). Accordingly, the first negative pixel voltage Vp1 and the second positive pixel voltage Vp2 are both capacitively affected by the third negative and positive polarity effective pixel signals -Vp and +Vp respectively applied to the second and third data lines (DL2) and (DL3), respectively, via the first and second parasitic capacitors Cdp1 and Cdp2, respectively, during the third horizontal period (H3). Since an absolute value of the third positive polarity effective pixel signal +Vp applied to the third data line (DL3) is relatively large, the capacitance of the second parasitic capacitor (Cdp2) is also relatively large, thereby positively decreasing the magnitude of the first negative pixel voltage Vp1 and positively increasing the magnitude of the second positive pixel voltage Vp2.

[0067] As can be seen from the discussion above, the various positive and negative polarity pixel signals, charged within each liquid crystal cell, capacitively

affect existing positive and negative pixel voltages, previously charged via the second and third data lines (DL2) and (DL3) through the first and second parasitic capacitors Cdp1 and Cdp2 within each liquid crystal cell. Moreover, due to the presence of the aforementioned polarity control signals (POL) applied to the second and third data lines (DL2) and (DL3), the polarity of the capacitance within the parasitic capacitors (Cdp1 and Cdp2) may be inverted during each horizontal period (H). As a result, the various pixel voltages charged within each liquid crystal cell may become offset from each other.

[0068] During, for example, the data apply period (DAP) of a first frame (1F), effective pixel signals may be applied to, for example, the second and third data lines (DL2 and DL3) in accordance with the dot inversion method. Due to the aforementioned offset, changes in first and second effective voltage (EVc and EVd) of the first and the second liquid crystal cells C and D, respectively, are substantially the same.

[0069] During the blanking period (BP) succeeding the data apply period (DAP), a dummy pixel signal having a negative polarity may be applied to the second data line DL2 while a dummy pixel signal having a positive polarity may be applied to the third data line DL3. In one aspect of the present invention, the negative polarity dummy pixel signal may include a white signal (WS). In another aspect of the present invention, the positive polarity dummy pixel signal may include a white signal

(WS). Subsequently, the second and third data lines DL2 and DL3 may be placed into a floating state. According to principles of the present invention, capacitance values of the first and second parasitic capacitors (Cpd1 and Cpd2), arranged within the first and second liquid crystal cells (C and D) and induced by the negative and positive polarity white signals (WS) applied to respective ones of the second and third data lines (DL2 and DL3), are substantially identical to each other, have inverted polarities, and are therefore offset. Since dummy pixel voltages associated with the first negative polarity dummy pixel signal (-Vp) and the second positive polarity dummy pixel signal (+Vp) are substantially identical, substantially no differences exist between the capacitive values of the first and second parasitic capacitors (Cdp1 and Cdp2). Accordingly, changes in the effective pixel voltages EVc and EVd, charged within the first and the second liquid crystal cells (C and D) during the blanking period, remain substantially the same during the blanking period (BP). Accordingly, generation of the horizontal stripe phenomenon may be substantially prevented.

[0070] Although the present invention have been described with respect to liquid crystal cells adjacent the second and third data lines and connected to the first and second gate lines, it will readily be appreciated that the principles of the present invention may be extended to all liquid crystal cells similarly arranged within the LCD panel 22. Moreover, and although the LCD display and method of driving the same has been described above in light of the dot inversion method, it will be readily

appreciated that the principles of the present invention may be readily extended to a column inversion method where polarities of pixel signals applied to adjacent ones of data lines are inverted, to an N-dot inversion method (N is an integer) where polarities of pixel signals applied between groups of liquid crystal cells are inverted. Regardless of the type of driving inversion method employed, dummy pixel signals representing substantially identical brightness levels may be applied to the data lines during the blanking period. Subsequently, the data lines may be placed into a floating state. Accordingly, deterioration of picture quality due to differences in capacitive coupling between vertically adjacent ones of liquid crystal cells may be prevented.

[0071] As described above, dummy pixel signals having substantially identical brightness levels may be provided to all data line during a blanking period. Subsequently, the data lines are placed in a floating state. Accordingly, differences in the effective pixel voltage of vertically adjacent pixels, due to differences in parasitic capacitor coupling between pixel signals charged to liquid crystal cells, can be minimized. As a result, deleterious generation of the horizontal stripe phenomenon may be substantially prevented, thereby improving a picture quality of the LCD device.

[0072] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or

scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.